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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| EXAMINER | |
|---|---|
| KANG, DONGHEE | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 11/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/730,636 | PEICHL ET AL. | |
| | Examiner | Art Unit | |
| | Donghee Kang | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12 and 14-19* is/are pending in the application.

4a) Of the above claim(s) *7,15,16 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-12,14,17 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/08/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election of embodiment 1 (Fig.1) in the reply filed on )9-02-04 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Claims 1-12 & 14-19 are pending in the present application. However, claims 7, 15-16 & 18 are withdrawn form further consideration.

### *Priority*

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Information Disclosure Statement*

3. Acknowledgment is made of receipt of applicant's Information Disclosure Statement (PTO-1449) field December 08, 2003.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4, 8, 10-12 & 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Calligaro (US 5,102,822).

Re claim 1, Calligaro teaches a method for manufacturing a PIN diode, comprising the following steps (Fig.1):

Forming a p-area (17, Fig.4) on a first surface of a wafer (2); forming an n-area on the first surface of the wafer spaced apart from the p-area; forming an intermediate area on the first surface of the wafer between the p-area and the n-area, wherein a doping concentration of the intermediate area is lower than a doping concentration of the p-area and lower than a doping concentration of the n-area; forming a first electrically conductive member (12) on a side of the p-area, which faces away from the intermediate area; and forming a second electrically conductive member (13) on a side of the n-area, which faces away from the intermediate area.

Re claim 2, Calligaro teaches providing the wafer and a device wafer; and wafer-bonding of the wafer and the device wafer, wherein the p-area, the n-area and the intermediate area are formed in the device wafer and insulated against the wafer.

Re claim 3, Calligaro teaches forming a trench in a section of the device wafer, which abuts on the intermediate area, wherein the trench extends from a surface of the device wafer, which faces away from the wafer, to a surface of the device wafer, which is opposite to the wafer; and filling the trench within insulating material (10).

Re claim 4, Calligaro teaches the trench is further formed in section of the device wafer, which abut on the p-area and on the n-area.

Re claim 8, Calligaro teaches a PIN diode comprising (Fig.1):

A p-area on a first surface of a wafer; an n-area on the first surface of the wafer; an intermediate area on the first surface of the wafer between the p-area and the n-area, wherein a doping concentration of the intermediate area is lower than a doping concentration of the p-area and lower than a doping concentration of the n-area.

Re claim 10, Calligaro teaches a trench in a section of the device wafer, which abuts on the intermediate area wherein the trench extends from a surface of the device wafer, which face away from the wafer, to a surface of the device wafer, which is opposite to the wafer, and wherein the trench is filled with an insulating material (10).

Re claim 11, Calligaro teaches the trench is arranged in section of the device wafer, which abut on the p-area and on the n-area.

Re claim 12, Calligaro teaches a shape of the intermediate area is rectangular, wherein the p-area and the n-area area arranged on two opposite sides of the intermediate area.

Re claim 14, Calligaro teaches at least either the p-area or n-area extend along width of the intermediate area.

6. Claims 1-2, 5-6, 8-9 & 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Cohen et al. (US 6,667,528).

Re claim 1, Cohen et al. teach a method for manufacturing a PIN diode, comprising the following steps (Fig.3C):

forming a p-area (7) on a first surface of a wafer (1); forming an n-area (6) on the first surface of the wafer spaced apart from the p-area; forming an intermediate area (5)

on the first surface of the wafer between the p-area and the n-area, wherein a doping concentration of the intermediate area is lower than a doping concentration of the p-area and lower than a doping concentration of the n-area; forming a first electrically conductive member (20) on a side of the p-area, which faces away from the intermediate area; and forming a second electrically conductive member (20) on a side of the n-area, which faces away from the intermediate area.

Re claim 2, Cohen et al. teach providing the wafer and a device wafer; and wafer-bonding of the wafer and the device wafer, wherein the p-area, the n-area and the intermediate area are formed in the device wafer and insulated against the wafer.

Re claim 5, Cohen et al. teach that the p-area or the n-area is formed by forming a trench in the device wafer and filling the same with p-doped or n-doped polysilicon, respectively.

Re claim 6, Cohen et al. teach the method further comprising the following step:

Forming an insulating layer (8) above the surface of the p-area, the n-area, and the intermediate area, which faces away from the first surface of the wafer (see fig.5).

Re claim 8, Cohen et al. teach a PIN diode comprising (Fig.3C):

A p-area on a first surface of a wafer; an n-area on the first surface of the wafer; an intermediate area on the first surface of the wafer between the p-area and the n-area, wherein a doping concentration of the intermediate area is lower than a doping concentration of the p-area and lower than a doping concentration of the n-area.

Re claim 9, Cohen et al. teach an insulating layer (4) on the wafer (1) and a device wafer on the insulating layer, wherein the p-area, the n-area, and the intermediate area are arranged in the device wafer.

Re claim 17, Cohen et al. teach the PIN diode further comprising an insulating layer (11, Fig.5), which covers surface of the p-area, the n-area, and the intermediate area, which face away from the wafer.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen et al. (US 6,667,528).

Cohen et al. do not explicitly teach the distance between the p-area and the n-area is more than 30 μm. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the distance of the intermediate layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

***Conclusion***

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 571-272-1656. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donghee Kang, Ph.D.
Primary Examiner
Art Unit 2811

dhk